REMARKS

Claims 1 and 9 were rejected under 35 U.S.C. 102(b) as being anticipated by Tomasz (US 6031878).

Claim 1 has been amended to recite: "an integrated circuit embodied on a single monolithic substrate" and "wherein analog and digital circuitry of both the tuning module and the several channel decoding modules are fabricated on that single monolithic substrate." The Examiner points to Tomasz col. 2, lines 59-62 which teaches that "the DBS signal delivered to the set-top box is ***directly converted*** from the received frequency ***to baseband***, in the preferred embodiment ***by a single integrated circuit***" (emphasis added). Thus, what Tomasz teaches is the use of a single integrated circuit to perform the function of direct conversion of the RF signal to baseband. This is supported by Tomasz Figure 2 and the integrated circuit 64 of the "tuner unit". The functionality performed on the "single integrated circuit" of Tomasz is only an analog downconversion and tuning functionality.

Applicants claim in claim 1 that both "the tuning module and the several channel decoding modules are fabricated on that single monolithic substrate." Thus, Applicants claim that the analog and digital circuitry of both "the tuning module and the several channel decoding modules" are fabricated on the same monolithic substrate. This is not, however, taught by Tomasz. In fact, Tomasz specifically teaches away from the claimed invention by providing an analog to digital converter unit 100 whose circuitry is fabricated on a ***separate*** integrated circuit substrate from substrate used for integrated circuit 64. Still further, Tomasz specifically teaches away from the claimed invention by providing a digital signal processing unit 78 whose circuitry is fabricated on a ***separate*** integrated circuit substrate from the substrate of integrated circuit 64.

Thus, Tomasz specifically teaches separating the analog functions of RF tuning and the digital functions of A/D conversion and digital signal processing by fabricating the associated circuitry on different integrated circuit substrates.

Applicants direct the Examiner's attention to Tomasz Figure 2 and reference, with respect to integrated circuit 64, the label "MAX2102." The reference "MAX2102" is an identification of an integrated circuit chip from MAXIM Integrated Products (MAXIM). Reproduced below is Figure 2 from the MAX2120 datasheet published by MAXIM. The Examiner will note the similarity to Figure 2 of the Tomasz reference.

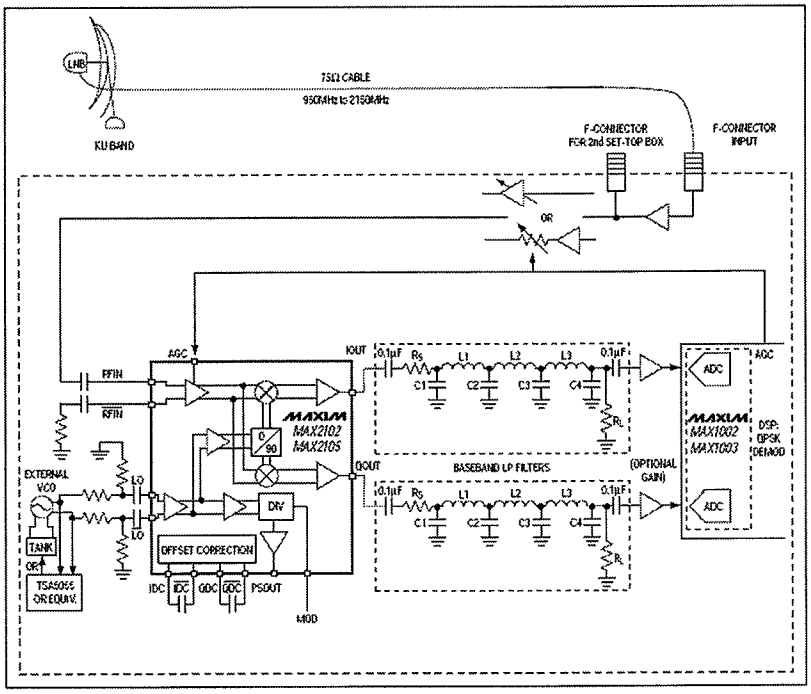

Figure 2. Typical Application

MAXIM 11

With respect to the analog to digital converter circuit, the Examiner will note the reference in the datasheet Figure 2 to "MAX1002" and "MAX1003." The Tomasz reference

makes mention in Figure 3 to "MAX1003/1004". The references "MAX1002," "MAX1003" and "MAX1004" are identifications of an integrated circuit chip family from MAXIM. The integrated circuits in this family are A/D converters which are fabricated on a separate monolithic substrate from the substrate use for the MAX2120 tuning circuit. There is no teaching or suggestion in Tomasz, or from MAXIM, for the integration of the circuitry for both the MAX2102 tuner and MAX1002/1003/1004 A/D converter onto a single substrate. The Tomasz reference itself further emphasizes the use of a separate integrated circuit substrate for the A/D converter (see, col. 4, lines 61-64).

With respect to the digital signal processor and the baseband digital processing circuitry, the MAX2120 datasheet published by MAXIM refers to the use of separate baseband integrated circuits (excerpt reproduced below).

- **Easy Interface to MAX1002/MAX1003 Dual ADC and Popular Baseband ICs**

The Tomasz reference further emphasizes the use of a separate integrated circuit, on a different substrate, for fabricating the baseband processing circuitry (col. 4, line 64 to col. 5, line 8).

It is thus clear that Tomasz fails to teach or suggest an integrated circuit embodied on a single monolithic substrate" and "wherein analog and digital circuitry of both the tuning module and the several channel decoding modules are fabricated on that single monolithic substrate" as claimed by Applicants. Claim 1 and its dependent claims are accordingly submitted to be patentable over the cited prior art.

The Examiner, on page 48, section 14, of the final Office Action, focus on the phrase "integrated circuit" and asserts that all circuitry of that integrated circuit would be on the same

substrate. Applicants do not disagree with the Examiner's statement, but assert that the Examiner has not considered the scope of the claim language and the teachings of the prior art. The Tomasz reference teaches associating certain circuitry with a certain integrated circuit. Thus only that circuitry, which in the case of the Tomasz teaching is the tuning circuitry, will be integrated and present on a single substrate. Other circuitry shown in Tomasz will either be not integrated at all (see, the discrete components of the baseband low-pass filter), or will be integrated on a separate (i.e., different) substrate. The claimed invention, however, specifically identifies the circuitry at issue which must be fabricated on a single integrated circuit substrate. In the case of the Tomasz reference, there is no teaching for the use of a single substrate onto which the recited circuitry of claim 1 has been integrated.

Claims 2, 10, 11, 13-15, 20, 38, 48-50 and 55 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins (US 6147713).

In claim 2, Applicants claim specific components of the tuning module. Again, the analog and digital circuitry associated with these components "are fabricated on that single monolithic substrate." Notably, Applicants specifically claim "a multibit analog/digital conversion stage." As discussed above, Tomasz specifically teaches the use of a separate integrated circuit chip (MAX1002) for the A/D converter. This chip and the tuning circuit chip do not share a common single monolithic substrate. Robbins likewise uses a DSP chip 12 on a substrate for digital processing which is separate from any analog tuning circuitry and its associated substrate (see, low IF in node 10). For these reasons alone, Claim 2 distinguishes over Tomasz.

Additionally, claim 2 recites "several digital devices for transposing frequencies that are connected to the output of the analog conversion stage, each digital device being configured to separately deliver a sampled digital signal centered at the zero frequency and corresponding to a selected channel." Again, the circuitry associated with these "several digital devices" must be "fabricated on that single monolithic substrate." As discussed above, Tomasz specifically teaches the use of a separate DSP and A/D converter integrated circuits. Robbins likewise uses a DSP chip 12 on a substrate for digital processing which is separate from any analog tuning circuitry and its associated substrate (see, low IF in node 10). For these reasons, Claim 2 further distinguishes over Tomasz.

Claim 2 further recites with the claimed several digital devices, "each digital device being configured to separately deliver a sampled digital signal centered at the zero frequency and corresponding to a selected channel." Robbins teaches only ONE digital device for transposing frequencies (see, DSP chip 12), and further there is only one output signal. Conversely, the claimed invention places several digital devices together and integrated on a common substrate, each of which delivering a sampled digital signal for a selected channel centered at zero frequency. This architecture, with at least two digital devices on a common substrate, is not taught by Tomasz or Robbins. For these reasons, Claim 2 further distinguishes over Tomasz.

Turning next to claim 10, Applicants claim "a first digital tuner that downconverts the digital signal to a first downconverted digital signal" and "a second digital tuner that downconverts the digital signal to a second downconverted digital signal." Applicants also claim "a first channel decoding digital module connected to the first digital tuner" and "a second channel decoding digital module connected to the second digital tuner." Applicants further claim

that the "circuitry of the converter, tuners and modules are fabricated on that single monolithic substrate."

While Tomasz teaches the use of a single IC for the tuner functionality (along with separate digital processing ICs), and while Robbins teaches a DSP IC 12 for video processing, there is no teaching or suggestion in the cited art for the use of a single integrated circuit substrate onto which are fabricated: an A/D converter, at least two distinct and separate zero-IF digital tuners, and at least two distinct and separate (as well as corresponding) channel decoding digital modules. There is no suggestion in the cited art for the integration of all these functionalities for fabrication on a "single monolithic substrate" as claimed. At best, the Tomasz and Robbins art cited by the Examiner teaches providing a multi-IC chip solution with a single tuner circuit and single digital processing circuit, each of those circuits being fabricated on a separate substrate. There is no suggestion in Tomasz or Robbins for plural zero-IF digital tuners fabricated on a common substrate, and further for plural channel decoders also fabricated on that same common substrate. Applicants accordingly submit that claim 10 and its dependent claims are patentable over the cited prior art.

Turning next to claim 38, Applicants note that claim 38 includes limitations similar to claim 1 and asserts that claim 38 is patentable over the cited prior art for at least the same reasons as claim 1. Claim 38 and its dependent claims are accordingly in condition for allowance.

Claims 7 and 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Lieber (US 5220164). Claims 7 and 8 are patentable over the cited prior art for at least the reasons recited above with respect to claim 1.

Claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Hwang (US 4894657). Claim 3 is patentable over the cited prior art for at least the reasons recited above with respect to claim 1. Applicants further submit that the circuitry associated with the digital decimator filter and digital error correction stage must be "fabricated on that single monolithic substrate." Tomasz, Robbins and Hwang all fail to teach or suggest integrating the claimed circuitry on a single substrate. For these reasons, Claim 3 further distinguishes over Tomasz.

Claims 4-6, 16-18 and 51-53 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins and Hwang. Claims 4-6, 16-18 and 51-53 are patentable over the cited prior art for at least the reasons recited above with respect to their respective base independent claims.

Claim 4 is further believed to distinguish over the cited prior art for at least the reasons recited above in connection with claim 2.

Claims 16-18 and 51-53 are further believed to distinguish over the cited prior art for at least the reasons recited above in connection with claim 3.

Claims 21-28, 30-32, 37, and 39-46 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins and Young (EP 0481543).

Claim 21 includes limitations similar to that of claim 10 and is asserted to be patentable over the cited prior art for at least the same reasons as claim 10. Again, the cited art fails to teach or suggest fabricating the circuitry of two A/D converters, two tuners and two digital decoders on a single substrate.

Claim 21 further recites "a first analog-to-digital converter" and "a second analog-to-digital converter." Outputs from the first and second A/D converters are provided to a "switching circuit that selectively couples the first and second digital signals output from the first and second converters to the first and second digital tuners." The Examiner points to switches 50 as taught by Young. These switches 50 function to selectively connect an input to the circuitry or alternatively connect a feedback loop from the output to the circuitry. This selective connection through switches 50 in Young is not material to the claimed invention.

In the claimed invention, there are two A/D converters and two digital processing modules. The claimed switching circuit functions to selectively couple the first and second digital signals output from the two A/D converters to the first and second digital tuners. Neither of the signals claimed is a feedback signal, but rather are both A/D converter outputs. The input signal versus feedback loop signal switching circuit taught by Young does not suggest the claimed switching circuit which interconnects two A/D converters and two digital processing modules in the manner claimed so that the output signals from the A/D converters can be selectively connected to the inputs of the digital tuners. The switching functionality taught by Young does not suggest an operation for selectively choosing the signal to be input for digital tuning from at least two possible A/D converter outputs. Likewise, the other art cited by the Examiner fails to teach or suggest such processing. Applicants accordingly submit that claim 21 and its dependent claims are patentable over the cited prior art.

Claims 40-46 are asserted to be patentable over the cited art for at least the reasons recited with respect to claim 21.

Claims 12 and 47 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins and Dapper (US 6275990). Claims 12 and 47 are patentable over the cited prior art for at least the reasons recited above with respect to their respective base independent claims.

Claims 19 and 54 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins and Lieber. Claims 19 and 54 are patentable over the cited prior art for at least the reasons recited above with respect to their respective base independent claims.

Claim 29 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins, Young and Dapper. Claim 29 is patentable over the cited prior art for at least the reasons recited above with respect to its independent base claim.

Claims 33-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins, Young and Hwang. Claims 33-35 are patentable over the cited prior art for at least the reasons recited above with respect to their base independent claim.

Claim 36 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Robbins, Young and Lieber. Claim 36 is patentable over the cited prior art for at least the reasons recited above with respect to its independent base claim.

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

Dated: May 22, 2008

Respectfully submitted,

By _____
Andre M. Szuwalski
Registration No.: 35,701
Gardere Wynne Sewell LLP
3000 Thanksgiving Tower
1601 Elm Street
Dallas, Texas 75201
(214) 999-4795
Attorneys For Applicant